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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WILLIAMS, KENT L	
ART UNIT	**PAPER NUMBER**
2139	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/749,035	SYDIR ET AL.	
	Examiner	Art Unit	
	Kent L. Williams	2139	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21 and 23-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21 and 23-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 February 2007 and 06 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9 March 2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-21 and 23-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Narad et al. (U.S. Patent No. 6,157,955).

C1. (Previously Presented) A network processor, comprising:

a crypto system **[**Figure 3, blocks 202 & 246.**]** ;

an alignment buffer to receive header data and ciphered data from the crypto system, the crypto system encrypting data to form ciphered data so that an intended receiver with a correct cryptographic key may decrypt the ciphered data **[**Column 24, Lines 50-65 *and* Column 7, Lines 5-6. The alignment buffer is considered an integral part of the "Crypto Coprocessor," which is in direct communication with the alignment buffer--(evidenced by Column 20, Lines 9-10 in tandem with Column 22, Lines 45-65).**]** ; and

a switch fabric having a plurality of transmit buffer elements to receive data from the alignment buffer, wherein the alignment buffer provides data to the switch fabric in blocks having a predetermined size **[**Column 9, Lines 45-63 *and* Column 24 & 25, Lines 65-67 & 1-11. The crypto processor(s)[1] has/have the data realigned (header/payload)

[1] Column 27, Lines 63-67.

using a buffer[2] after cryptographic processing[3] that is then sent to the transmit buffer to be sent via switch fabric and an interface[4] in predetermined sizes,[5] where it is understood that data having had a cryptographic process performed thereon will be "ciphered data."].

C2. (Previously Presented) The network processor according to claim 1, further including an interface to transmit data from the switch fabric [Figure 3, blocks 248 & 218.]

C3. (Original) The network processor according to claim 2, wherein the interface includes a SPI4 type interface [Column 1, Lines 50-65. Teaching "Network Interface Controllers" (NIC) anticipates both SPI4 and NPSI (as they are differing network interfaces). Please see the two NIC specification sheets for SPI4 and NPSI for verification regarding the aforementioned assertion.].

C4. (Original) The network processor according to claim 2, wherein the interface includes art NPSI interface [Rejected per claim 3.].

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[2] Column 20, Lines 9-10.
[3] Column 7, Lines 5-6.
[4] Column 25, Lines 45, 46 & 50; and Column 32, Lines 18-25.
[5] Column 8, Lines 28-30.

C5. (Original) The network processor according to claim 1, wherein the crypto system includes first and second crypto units [Column 27, Lines 58-67.].

C6. (Original) The network processor according to claim 1, wherein the crypto system includes a predetermined number of crypto unit processing contexts and the alignment buffer includes a buffer element for each of the predetermined number of processing contexts [The Examiner has taken and upholds Official Notice on processing contexts (as outlined by the prosecution history—Office Actions mailed 20 December and 28 March 2007). The buffer elements inherently can only be used by one context at a time (outlined in Column 20, Lines 15-24).].

C7. (Original) The network processor according to claim 6, wherein the crypto system includes a plurality of cipher cores [Column 27, Lines 58-67 *and* Column 9, Lines 5-11, where the Examiner understands each function to require specialized logic that is commonly referred to as a "core" within the context of a *cryptographic* processor. Teaching "Crypto Daughtercard," as taught within Columns 13 & 17, Lines 12 & 23, anticipates cryptographic processors (or "crypto units") with a plurality of cipher cores for varying crypto algorithms. A "core," per page 3 of the instant application specification, is defined as an algorithm implemented in hardware.].

C8. (Original) The network processor according to claim 7, wherein the plurality of cipher cores correspond to a plurality of cipher algorithms [Rejected per claim 7.].

C9. (Currently Amended) A method of processing data in a device having at least one crypto unit, comprising:

storing a portion of a packet header in an alignment buffer that has a first storage size [Figure 9.];

storing a first portion of a first data block of ciphered data from the at least one crypto unit in the alignment buffer, the at least one crypto unit encrypting data to form the ciphered data so that an intended receiver with a correct cryptographic key may decrypt the ciphered data [Figure 9 in light of Figure 3, blocks 246 & 202.];

transmitting the ciphered data from the alignment buffer to a first buffer element in a switch fabric interface unit [Column 27, Lines 10-25. The alignment buffer is considered an integral part of the "Crypto Coprocessor," which is in direct communication with the alignment buffer-- (evidenced by Column 20, Lines 9-10 in tandem with Column 22, Lines 45-65).];

transmitting further data blocks of the ciphered data from the alignment buffer to the first buffer element until the first buffer element is full;

allocating a second buffer element in the switch fabric interface unit; and

transmitting the ciphered data in the alignment buffer to the second buffer element [Column 29 & 30, Lines 57-67 & 1-40.].

C10. (Currently Amended) The method according to claim 9, further including transmitting the ciphered data from the at least one crypto unit to a selected one of a plurality of elements in the alignment buffer [Column 29 & 30, Lines 57-67 & 1-40.].

C11. (Original) The method according to claim 9, wherein the alignment buffer includes a number of buffer elements corresponding to a number of processing contexts for the at least one crypto unit [Rejected per claim 6.].

C12. (Currently Amended) The method according to claim 9, further including transmitting the ciphered data from the switch fabric interface unit over an interface [Rejected per claim 2.].

C13. (Currently Amended) The method according to claim 12, further including transmitting the ciphered data from the switch fabric interface unit over an SPI4 interface [Rejected per claim 3.].

C14. (Currently Amended) The method according to claim 9, further including transmitting the ciphered data from the switch fabric interface unit over an NPSI interface [Rejected per claim 3.].

C15. (Currently Amended) The method according to claim 9, further including transmitting the ciphered data from the alignment buffer in an amount that is a multiple

of a predetermined number of bytes [Column 8, Lines 28-30.].

C16. (Original) The method according to claim 15, wherein the predetermined number of bytes is 16 [Rejected per claim 15. Please see MPEP 2144.04, subsection 4A.].

C17. (Currently Amended) The method according to claim 9, further comprising including transmitting the ciphered data to the second buffer element in an amount less than the predetermined number of bytes for an end of packet [Column 33, Lines 20-26.].

C18. (Currently Amended) A ~~network~~ processor disposed on ~~an~~ integrated circuit, comprising:

first and second crypto units each having a plurality of cipher cores and a predetermined number of processing contexts, the first and second crypto units encrypting data to form ciphered data so that an intended receiver with a correct cryptographic key may decrypt the ciphered data [Column 27, Lines 58-67 *and* Figure 9 in light of Figure 3, blocks 246 & 202, where processing contexts rejected per claim 6.];

an alignment buffer having a respective element for each of the plurality of processing contexts to receive the ciphered data from the first and second crypto units [Column 19 & 20, Lines 63-67 & 1-10 in light of Column 23, Lines 9-14. The alignment buffer is considered an integral part of the "Crypto Coprocessor," which is in direct communication with the alignment buffer-- (evidenced by Column 20, Lines 9-10 in

tandem with Column 22, Lines 45-65).];

a media switch fabric interface unit having a plurality of transmit buffer elements to receive the ciphered data from the alignment buffer in an amount that is a multiple of a predetermined number of bytes [Column 29 & 30, Lines 57-67 & 1-40 *and* Column 8, Lines 28-30.]; and

an interface to transmit the ciphered data from the media switch fabric [Figure 3, blocks 248 & 218.].

C19. (Currently Amended) The ~~network~~ processor according to claim 18, wherein the interface includes an SPI4 interface [Rejected per claim 3.].

C20. (Currently Amended) The ~~network~~ processor according to claim 18, wherein the interface includes an NPSI interface [Rejected per claim 3.].

C21. (Currently Amended) A network switching device, comprising

a network processor disposed on an integrated circuit comprising: ~~including~~

a crypto system, the crypto system encrypting data to form ciphered data so that an intended receiver with a correct cryptographic key may decrypt the ciphered data, the crypto system includes a predetermined number of crypto unit processing contexts and the alignment buffer includes a buffer element for each of the predetermined number of processing contexts [Figure 3, blocks 202 & 246 *and* Column 24, Lines 50-65 *and* Column 7, Lines 5-6 *and* Column 19 & 20, Lines 63-67 & 1-10 in light of Column 23,

Lines 9-14.];

an alignment buffer to receive header data and the ciphered data from the crypto system [Column 24, Lines 50-65 *and* Column 7, Lines 5-6. The alignment buffer is considered an integral part of the "Crypto Coprocessor," which is in direct communication with the alignment buffer-- (evidenced by Column 20, Lines 9-10 in tandem with Column 22, Lines 45-65).]; and

a switch fabric interface unit having a plurality of transmit buffer elements to receive the ciphered data from the alignment buffer, wherein the alignment buffer provides the ciphered data to the switch fabric in blocks having a predetermined size [Column 29 & 30, Lines 57-67 & 1-40 *and* Column 8, Lines 28-30.].

C22. (Cancelled)

C23. (Original) The device according to claim 21, wherein the crypto system includes a plurality of cipher cores, wherein the plurality of cipher cores correspond to a plurality of cipher algorithms [Rejected per claim 7.].

C24. (Original) The device according to claim 21, wherein the device includes a router [Column 3, Lines 8-42.].

C25. (Currently Amended) A network, comprising:

a network switching device including a ~~network~~ processor disposed on an integrated

circuit comprising:

a crypto system, the crypto system encrypting data to form ciphered data so that an intended receiver with a correct cryptographic key may decrypt the ciphered data [Column 7, Lines 4-6.];

an alignment buffer to receive header data and the ciphered data from the crypto system [Column 24, Lines 50-65. The alignment buffer is considered an integral part of the "Crypto Coprocessor," which is in direct communication with the alignment buffer--(evidenced by Column 20, Lines 9-10 in tandem with Column 22, Lines 45-65).]; and

a switch fabric interface unit having a plurality of transmit buffer elements to receive the ciphered data from the alignment buffer, wherein the alignment buffer provides the ciphered data to the switch fabric in blocks having a predetermined size [Column 9, Lines 45-63, and the data size taught in Column 8, Lines 28-30.].

C26. (Original) The network according to claim 25, wherein the crypto system includes a predetermined number of crypto unit processing contexts and the alignment buffer includes a buffer for each of the predetermined number of processing contexts [Rejected per claim 6.].

C27. (Original) The network according to claim 26, wherein the crypto system includes a plurality of cipher cores [Rejected per claim 7.].

C28. (Original) The network according to claim 25, wherein the network switching device corresponds to a router [Column 3, Lines 8-42.].

Response to Arguments

3. Applicant's arguments, see remarks, filed 30 April 2007, with respect to the interview summary, mailed 9 March 2007, have been fully considered and are persuasive. All of the previous rejections (and objections) of the Office Action, mailed 28 March 2007, have been withdrawn.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kent L. Williams whose telephone number is 571-270-1376. The examiner can normally be reached on Mon-Fri 7:00-4:30 with Alternate Fridays Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz R. Sheikh can be reached on 571-272-3795. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Kent Williams
5/31/2007

CHRISTOPHER REVAK
PRIMARY EXAMINER